RQ56-200G-FR4

200G QSFP56 FR4 2KM LC Optical Transceiver

The 200G QSFP56 FR4 Transceiver is designed to transmit and receive optical data links 50 Gb/s bit rate per channel with PAM4 modulation format via up to 2km single mode fiber. It is hot pluggable transceiver with QSFP56 package. The module comprises high performance LD PIN DSP etc.

Features

- Up to 50Gbps data rate per channel by PAM4 modulation
- 4 duplex channels transmitters and receivers
- Integrated CWDM LD and PD array
- LC/UPC connecting interface compliant
- Single +3.3V power supply
- DDM function implemented
- Hot-pluggable QSFP56 form factor
- Transmission length up to 2km
- Low power dissipation:<6.5w
- International class 1 laser safety certified
- Operating temperature range: 0℃ ~ +70 ℃
- Compliant with ROHS10

Applications

- 200GBASE-FR4 Ethernet
- Switch & Router Connections
- Data Centers
- Other 200G Interconnect Requirements.

Standards

- IEEE 802.3cd
- CMIS Rev 4.0
- OIF-CEI-04.0 56G-VSR-PAM4
- IEEE 802.3bs Annex120E
- SFF-8024 Rev. 4.6
- SFF-8679 Rev1.8
- SFF-8665 Rev1.9

Specifications

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter (per Lane)						
Signaling Speed per Lane		GBd		26.5625		
Modulation format				PAM4		
Center wavelength	WL	nm	1264.5	1271	1277.5	
			1284.5	1291	1297.5	
			1304.5	1311	1317.5	
			1324.5	1331	1337.5	
Side-mode suppression ratio	SMSR	dB	30			
Average Launch Power per Lane	TXPx	dBm	-4.2		4.7	
Tx OMA per lane	TXOMA	dBm	-1.2		4.5	
Optical Extinction Ratio	ER	dB	3.5			
Transmitter and dispersion eye closure for PAM4 per Lane	TDECQ	dB			3.3	
Optical return loss tolerance	ORL	dB			16.5	
Relative Intensity Noise	RIN	dB/Hz			-132	
Receiver (per lane)						
Signaling Speed per Lane				26.5625		
Center wavelength	WL	nm	1264.5	1271	1277.5	
			1284.5	1291	1297.5	
			1304.5	1311	1317.5	
			1324.5	1331	1337.5	
Damage Threshold	DT	dBm	5.7			
Average Launch Power per Lane	RXP	dBm	-8.2		4.7	
Receiver reflectance	Rfl	dB			-26	
Difference in receive power between any two lanes		dB			4.1	
Receiver sensitivity (OMA outer)		dBm			-6	
Stressed receiver sensitivity (OMA outer)		dBm			-3.6	

Ordering Information

PN	Package	Data rate	Laser	Detector	Temp	Reach	Others	Application
RQ56-200G-FR4	QSFP56	200G	DFB	PIN	0~70 ℃	2km	RoHS	200G Base FR4

PN	RQ56-200G-FR4
Description	200G Base FR4 Transceiver -CT
SAP No	-
Customer PN	-

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	℃	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	Vcc	V	-0.5	+4.0

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tc	oC	0	/	70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465
Baud Rate (Per channel)	BR	GBd		26.5625	

Optical Interface

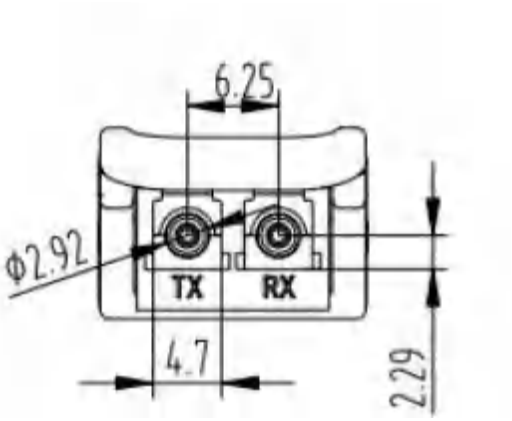


Figure 1. Optical interface

Note： Optical interface shown in figure 1.

Principle diagram

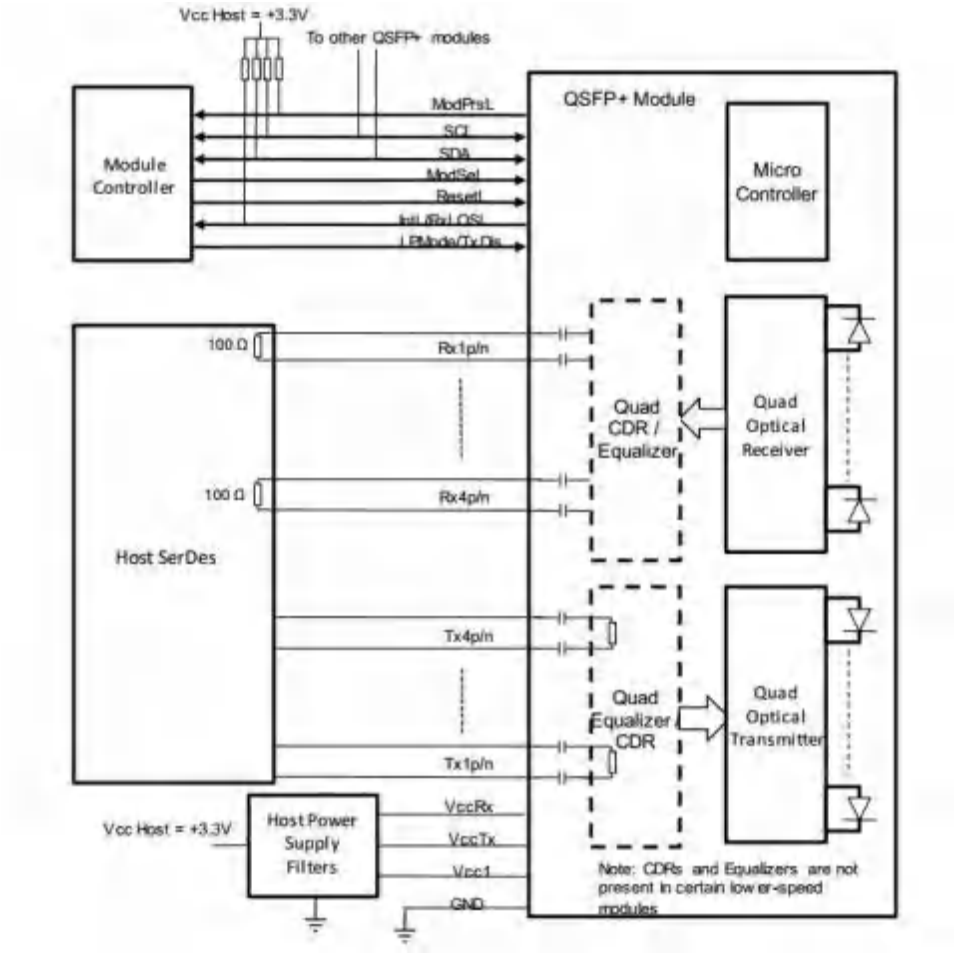


Figure 2. Module Principle Diagram

Electric Ports Definition

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Supply Voltage	VCC VCC3.3-Tx VCC3.3-Rx	V	3.135	3.3	3.465	
Power Consumption	Pc	W			6.5	
Transceiver Power-on Initialize Time		ms			2000	
Transmitter						
Differential peak-to-peak input voltage tolerance		mV	900			
Differential termination mismatch		%			10	
Differential input return loss(SDD11)		dB			See CEI-56G -VSR	

Common-mode to differential conversion and differential to common-mode conversion (SCD11,SDC11)		dB			See CEI-56G -VSR	
Receiver						
Differential peak-to-peak output voltage		mV			900	
DC Common Mode Voltage	Vcm	mV	-0.35		2.85	
AC Common Mode Noise, RMS		mV			17.5	
Differential termination mismatch		%			10	
Differential output return loss (SDD22)		dB			See CEI-56G -VSR	
Common-mode to differential conversion and differential to common-mode conversion (SCD22, SDC22)		dB			See CEI-56G -VSR	
IIC communication						
IIC Clock frequency	-	KHZ	/	400	1000	
clock stretching	-	us	/	/	500	
Data hold time	-	ns	/	/	/	

Pin Description

PIN	Logic	Symbol	DESCRIPTION	NOTE
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCOMS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-0	Rx3p	Receiver Non-Inverted Data Output	
15	CML-0	Rx3n	Receiver Inverted Data Output	

16		GND	Ground	1
17	CML-0	Rx1p	Receiver Non-Inverted Data Output	
18	CML-0	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-0	Rx2n	Receiver Inverted Data Output	
22	CML-0	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-0	Rx4n	Receiver Inverted Data Output	
25	CML-0	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-0	Mod PrsL	Module Present	
28	LVTTL-0	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636)	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636).	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Input	
34	CML-I	Tx3n	Transmitter Non-Inverted Data output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Input	
37	CML-I	Tx1n	Transmitter Non-Inverted Data output	
38		GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP56 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the module in any combination.

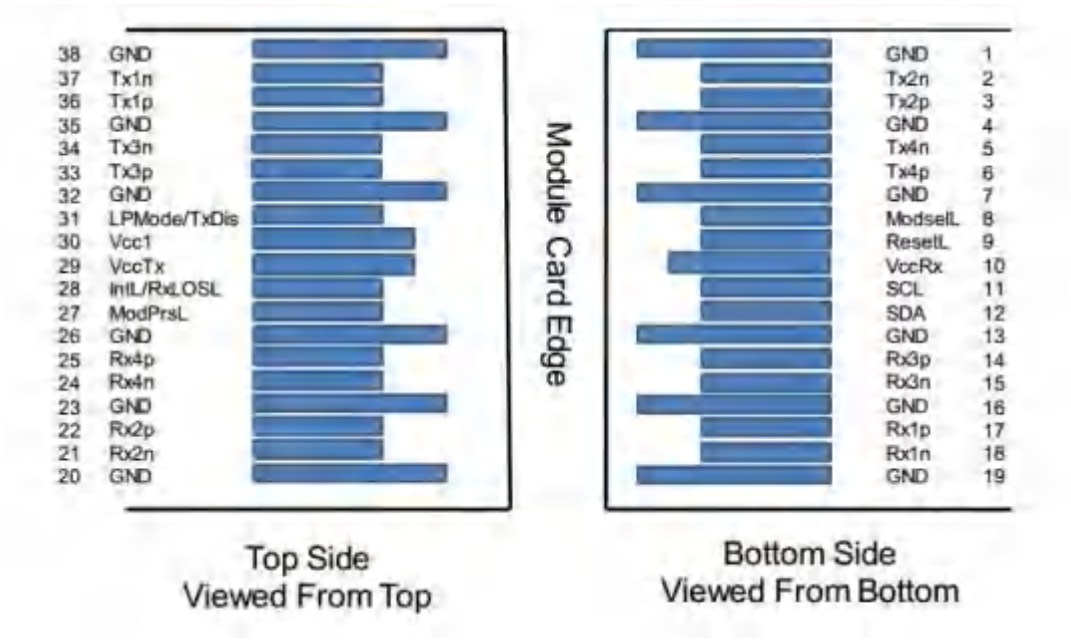
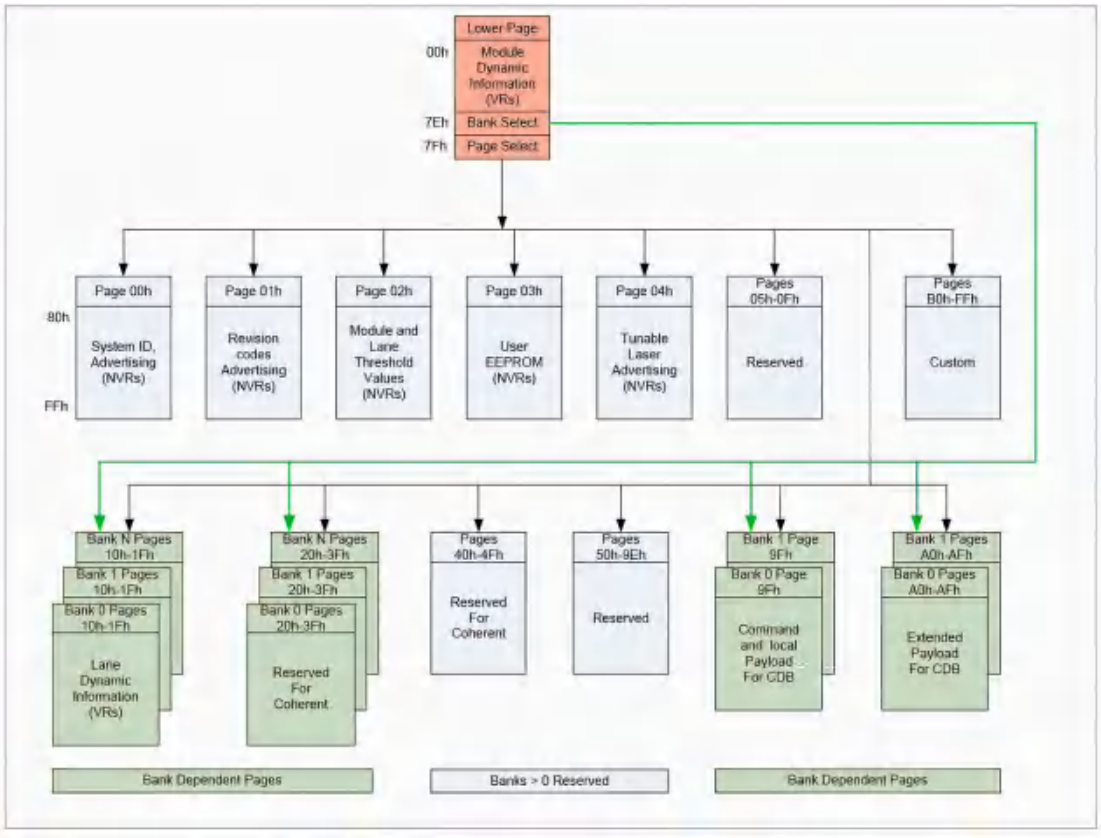


Figure 3. Electrical Pin-out Details

Module Memory Map



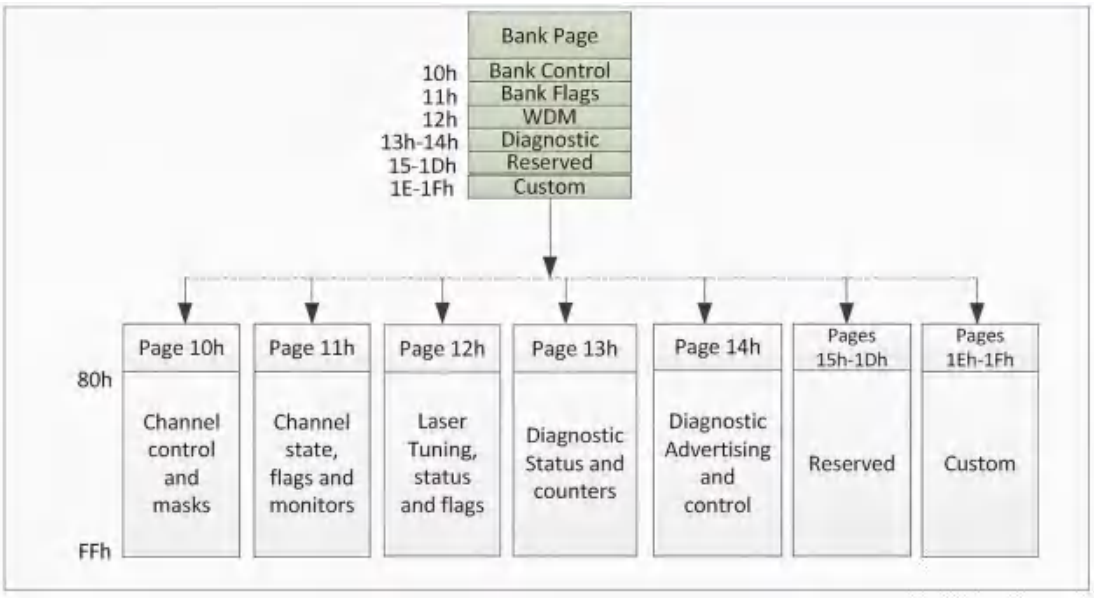


Figure 4 Digital Diagnostic Memory Map

Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC resistance of less than 0.1Ω should be used in order to maintain the required voltage at the host edge card connector. It is recommended that the 22 uF capacitors each have an equivalent series resistance of 0.22Ω. The specification of the host power supply filtering network is beyond the scope of this specification, particularly because of the wide range of QSFP56 module Power Classes. Figure is the suggested transceiver/host interface.

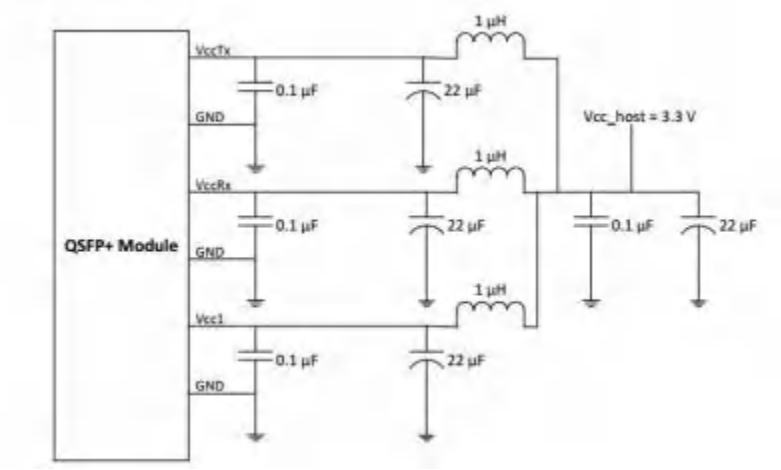


Figure 5 Recommended Host Board Power Supply Filtering

Package Outline

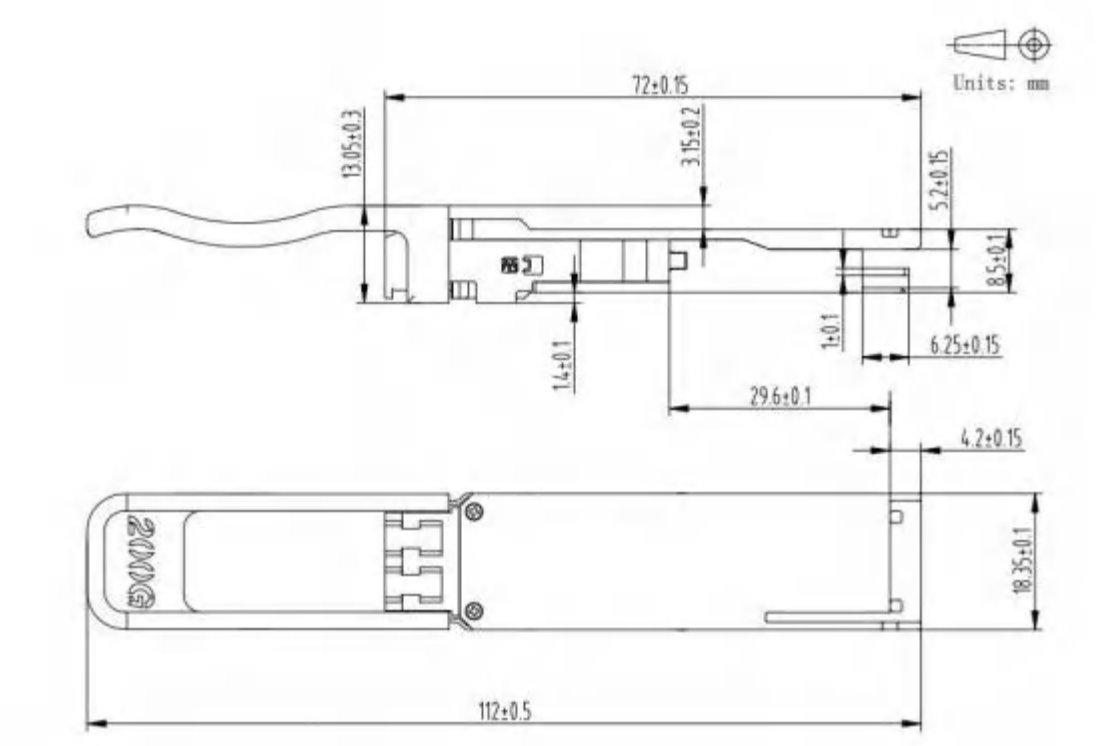


Figure 6 Package Outline