400G OSFP DR4 Specification

Features

- Form Factor: Hot-pluggable OSFP form factor
- Data Rate: Aggregate data rate of 425 Gb/s and Breakout data rate of 106.25 Gb/s
- Optical Interface: Compliant to 400GBASE-DR4 and 4x100GBASE-DR
- Transmitter: EML 1310nm transmitter
- Electrical Interface: Compliant to 400GAUI-4 and 4x100GAUI-1
- Receiver: PIN and TIA array on the receiver side
- Management Interface: I2C management interface
- Reach: Up to 500m over MPO-12/APC single mode fiber
- Power consumption: 9 W max
- Operating case temperature: 0 ~ 70 ℃
- Power Supply: Single 3.3V power supply

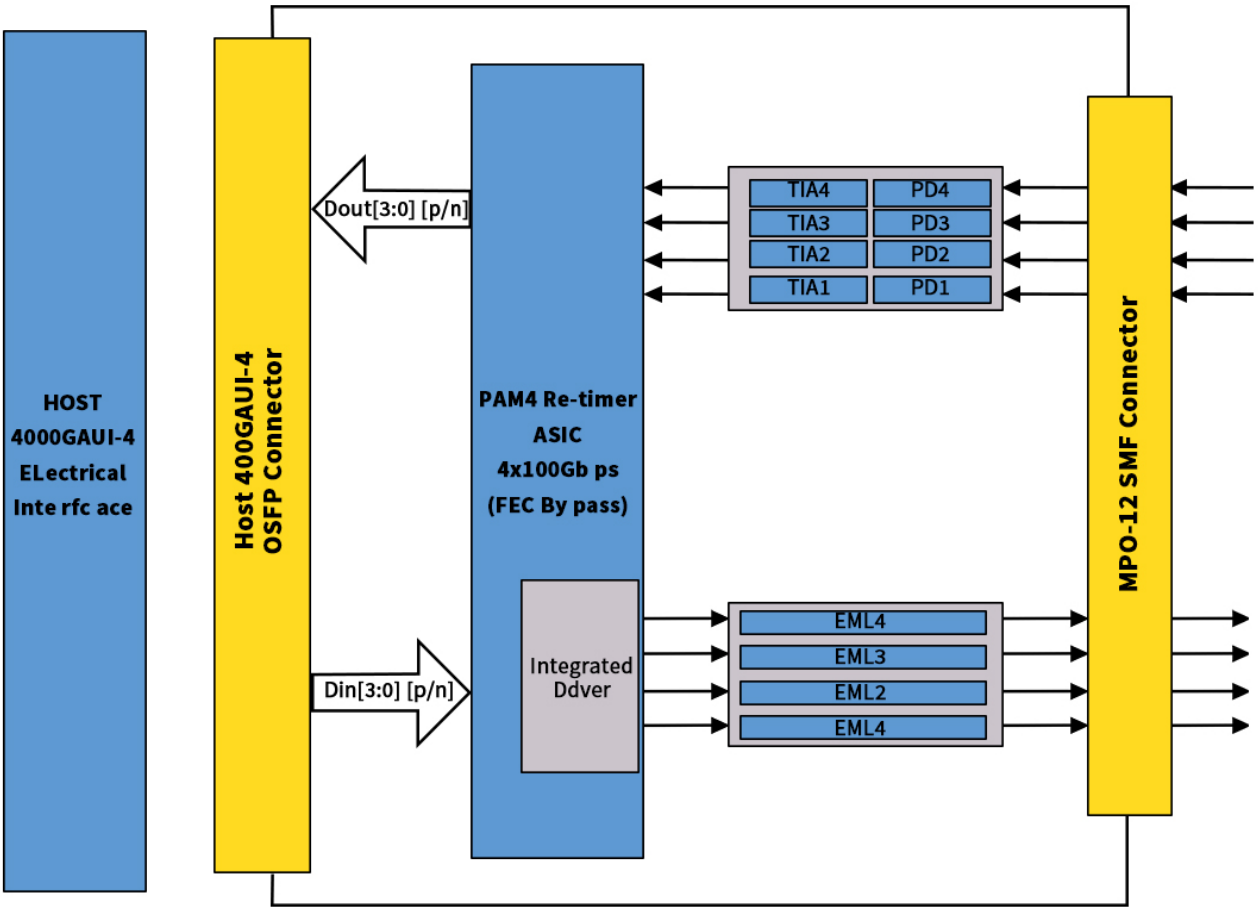
Compliance

- Form Factor: OSFP MSA
- Optical: IEEE802.3bs Electrical: IEEE802.3ck Firmware: CMIS
- Environment: RoHS
- Stability: GR-468-CORE

Applications

- 400Gb/s Ethernet
- Data Center
- InfiniBand

Functional Block Diagram



1. General Description

The 400G OSFP DR4 are high performance, cost effective transceivers designed for utilization in 400 Gigabit Ethernet links over 500 meters of singe mode fiber. On transmitter side, the module converts four channels of 53.125 GBaud (PAM4) electrical data to four channels of parallel optical signals with data rate of 53.125 GBaud (PAM4). At receiver side, the module converts four channels of parallel optical signals with data rate of 53.125 GBaud (PAM4) into four channels of 53.125 GBaud (PAM4) electrical output data.

The product is designed according to the OSFP MSA. It is designed to meet the harshest external operating conditions including temperature, humidity, and EMI interference.

2. Absolute Maximum Ratings and Recommended Operating Conditions

（Table 2.1 Absolute Maximum Ratings）

Parameter	Symbol	Min	Typical	Max	Unit
Storage Temperature	Ts	-40		85	°C
Storage Relative Humidity (non-condensation)	RH	5		95	%
Supply Voltage	Vcc	-0.5		3.6	V
Supply Voltage	PIN			5.0	dBm

（Table 2.2 Recommended Operating Conditions）

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	TC	0		70	°C
Signaling Rate, each lane			53.125		GBd
Data Rate Accuracy		-100		100	ppm
Power Supply Voltage	Vcc	-3.135	3.3	3.465	V
Pre-FEC Bit Error Ratio				2.4E-4	
Transmission Distance				500	m

3.Optical Specification

3.1 Optical Transmitter

（Table 3.1 Transmitter Optical Interface）

Parameter	Symbol	Min	Typical	Max	Unit
Signaling rate, each lane	SR	53.125+/-100ppm			GBd
Modulation format		PAM4			
Lane wavelength	λ	1304.5	1311.0	1317.5	nm
Side-mode suppression ratio	SMSR	30			dB
Average launch power, each lane[a]	AOP_{TX}	-2.9		4.0	dBm
Outer Optical Modulation Amplitude (OMAouter), each lane[b]	OMA_{TX}	-0.8		4.2	dBm

Launch power in OMAouter minus TDECQ, each lane		-2.2			dBm
Transmitter eye closure for PAM4 (TECQ), each lane	TECQ			3.4	dB
Average launch power of OFF transmitter, each lane	AOP_{OFF}			-15	dB
Extinction ratio, each lane	ER	3.5			dB
$RIN_{21.4}OMA$				-136	dB/Hz
Optical return loss tolerance	RLTol			21.4	dB
Transmitter reflectance[c]	Reflectance_ Tx			-26	dB

Notes:

a. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

b. Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed these values.

c. Transmitter reflectance is defined looking into the transmitter.

3.2 Optical Receiver

(Table 3.2 Receiver Optical Interface)

Parameter	Symbol	Min	Typical	Max	Unit
Signaling rate, each lane	SR	53.125	53.125+/-100ppm		GBd
Modulation format		PAM4			
Lane wavelengths	λ	1304.5	1311.0	1317.5	nm
Damage threshold, each lane[a]	DThd	5			dBm
Average receive power, each lane[b]	AOP_{RX}	-5.9		4	dBm
Receive power (OMAouter), each lane	OMARX			4.2	dBm
Receiver reflectance	Reflectance_Rx			-26	dB
Receiver sensitivity (OMAouter), each lane[c]	RxSens			-4.4	dBm
Stressed receiver sensitivity (OMAouter), each lane[d]	SRS			-1.9	dBm
Conditions of stressed receiver sensitivity test:[e]					
Stressed eye closure for PAM4 (SECQ), lane under test			3.4		dB

OMAouter of each aggressor lane				4.2		dBm
Rx LOS	LOS Assert		-15			dBm
	LOS De-assert				-7.5	dBm
	LOS Hysteresis		0.5		5	dB

Note:

a. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.

b. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

c. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.

d. Measured with conformance test signal at TP3 for the BER = 2.4E-4. e. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

4.Electrical Specification

4.1 Electrical Specifications

(Table 4.1 Module input characteristics)

Parameter	Test Point	Min	Typical	Max	Unit
Signaling rate, each lane	TP1	53.125 ± 100 ppm			GBd
Differential pk-pk voltage tolerance	TP1a	750			mV
Peak-to-peak AC common-mode voltage tolerance	TP1a	25			mV
Differential-mode to common-mode return loss, RLcd	TP1	Equation (120G–2)			dB
Effective return loss, ERL	TP1	8.5			dB

Differential termination mismatch	TP1			10	%
Module stressed input tolerance	TP1a	See 120G.3.4.3			-
Single-ended voltage tolerance range	TP1a	–0.4		3.3	V
DC common-mode voltage tolerance	TP1	-0.35		2.85	V
Module stressed input tolerance test :					
Pattern generator transition time	TP1a		9		ps
Applied peak-peak sinusoidal jitter	TP1a		Table 162-16		
Eye height	TP1a		10		mV
Vertical eye closure, VEC	TP1a	12		12.5	dB
Crosstalk differential peak-to-peak voltage	TP4		845		mV
Crosstalk transition time	TP4		8.5		ps

(Module output characteristics at TP4)

Parameter	Test Point	Min	Typical	Max	Unit
Signaling rate, each lane	TP4	53.125 ± 100 ppm			GBd
Peak-to-peak AC common-mode voltage tolerance	TP4			25	mV
Differential peak-to-peak output voltage Short mode Long mode	TP4			600 845	mV
Eye height	TP4	15			mV
Vertical eye closure, VEC	TP4			12	dB
Common-mode to differential-mode return loss, RLdc	TP4	Equation (120G–1)			dB
Effective return loss, ERL	TP4	8.5			dB
Differential termination mismatch	TP4			10	%
Transition time	TP4	8.5			ps
DC common-mode voltage tolerance	TP4	-0.35		2.85	V

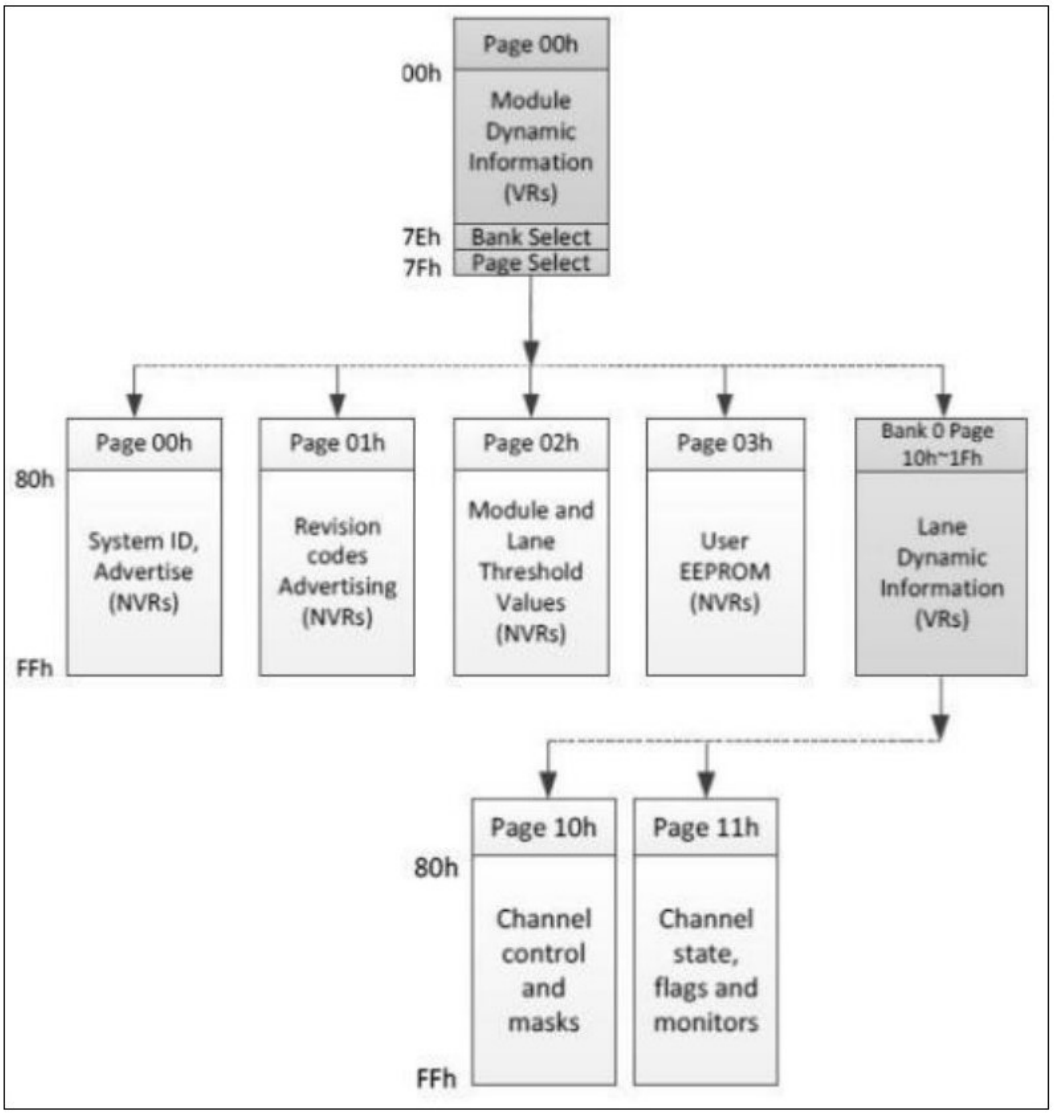
4.2 Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

Parameter	Accuracy	Unit
Internally Measured Transceiver Temperature	+/-3	℃
Internally Measured Transceiver Supply Voltage	+/-3	%
Measured Tx Bias Current	+/-10	%
Measured Tx Output Power	+/-3	dB
Measured Rx Received Average Optical Power	+/-3	dB

5.User Interface

The memory map follows CMIS and is described as follows:



(Figure 5.1 Simplified CMIS Module Memory Map Architecture)

6. Pin Assignment and Description

The OSFP module pinout and connector pin list are as follows:

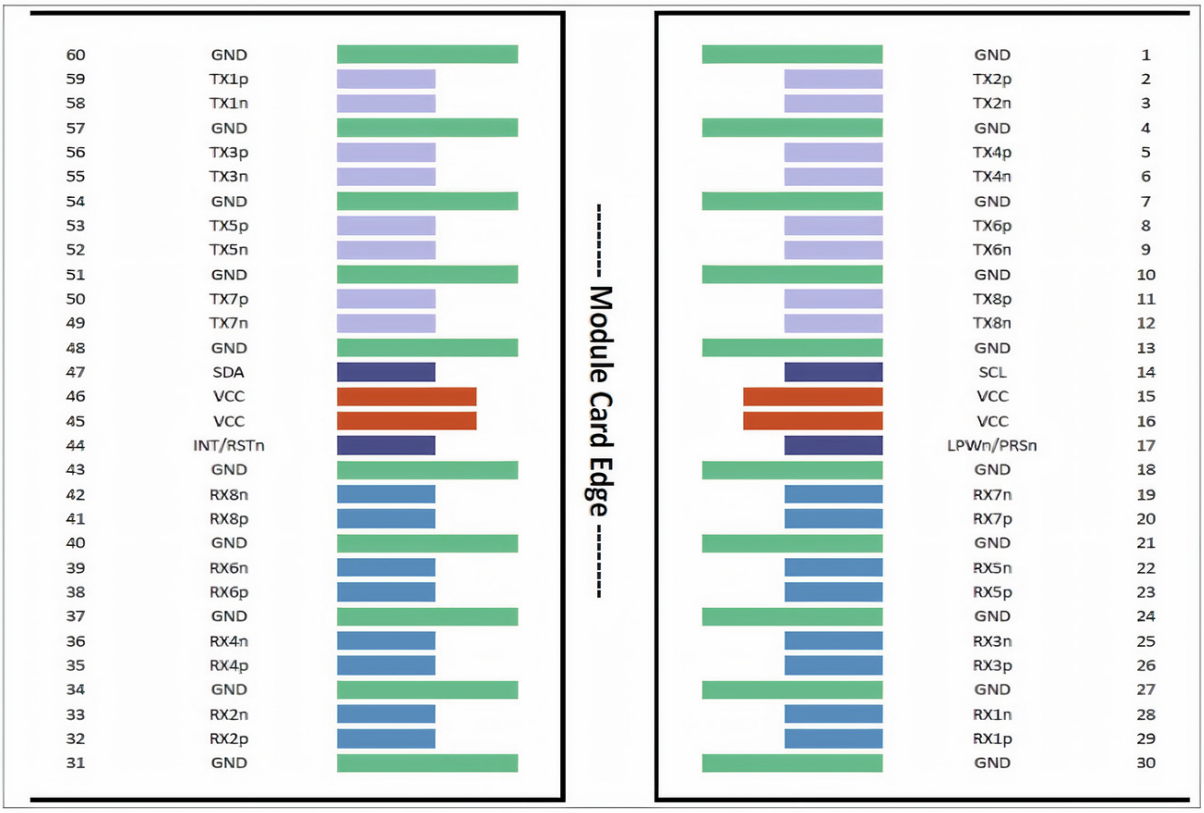


Figure 6.1 OSFP module pinout

6.2 Pin Description

(Table 6.2 Pin Description)

Pin	Name	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	Tx2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	Tx2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	Tx4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	Tx4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	Tx6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	Tx6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	

12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directiona	3	Open-Drain with pullup resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn[2]	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required

						circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pullup resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Notes:

1. Plug Sequence specifies the mating sequence of the host connector and module. The contact sequence is 1,2,3.
2. LPWn/PRSn is a Multi-level signal for low power control from host to module and module presence indication from module to host. It designed according to OSFP Module Specification Section 13.5.3.
3. INT/RSTn is a Multi-level signal for interrupt request from module to host and reset control from host to module. It designed according to OSFP Module Specification Section 13.5.2.

7. Package Dimensions

Package dimensions in mm are specified in OSFP OSFP MSA.

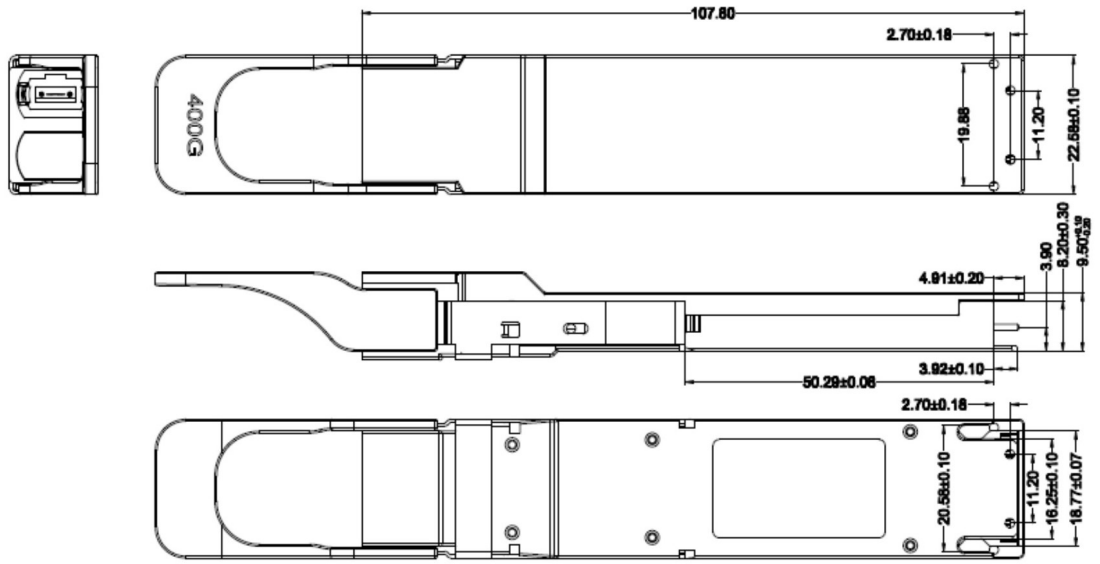


Figure 7.1 Package dimensions

9. Ordering Information

Part Number	Temperature Range	Distance	Fiber Type	E/O	O/E	Media Connector
R12OSFP-400G-DR4	0 to 70℃	500m	SMF	EML 1310nm	PIN	MPO12